Computing Reviews	477		Association for Computing Machinery
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Review		Search	\bigcirc
Democratizing domain-specific computin Chi Y., Chi Y., Qiao W., Qiao W., Sohrabizadeh J., Cong J. Communications of the ACM66 (1)	A., Sohrabizadeh A., W		
Date Reviewed: Jun 22 2023		(Full Text)	
As computer professionals, we mostly envision default. Over the past decades, Moore's law a given us consistently better "toys": faster cort tools, computer science has changed the face professionals focus on building software. Can specific accelerators (DSAs), that is, purpose- circuits, ASICs) that, at the cost of losing gen and energy efficiency than general-purpose c The authors' main focus is to present AutoDS	nd Dennard scaling hav nputers, larger storage of humankind. Howeve software developers wo built computers (applic terality, can deliver muc hips? E, a design-space explo	Related TopicsBrowseAlertsGeneral (D.0.)(Add)General (D.1)(Add)General (D.3.0.)(Add)Manage AlertsMore Alerts	
in order to present it some more background Of course, the authors start by acknowledgine expensive for most use cases, in no small par focus, however, on field-programmable gate a be reconfigured to perform as DSAs. Althougl ASICs, the authors argue that they can bring computing, accelerating workloads tens or hu central processing units (CPUs) to tackle ther	g that designing ASICs of t due to the cost of chip arrays (FPGAs), a specia n FPGAs are not as fast many of the advantage ndreds of times compan	o manufacturing. They al kind of chip that can as manufactured s of purpose-specific	
The authors acknowledge the first hurdle for programmers used to dealing with regular programming: the completely unfamiliar developing environment, based on hardware description languages such as Verilog or VHDL, which are very different from the languages they use for the bulk of their day-to-day work. Different FPGA vendors offer high-level synthesis (HLS) tools so that FPGAs can be programmed using a more familiar $C/C++/OpenCL$ program, annotated with "pragmas" to specify the compiler to use for specific parallelization, pipelining, buffering, and others. The correct use of such pragmas results in the same code being compiled to an FPGA able to solve a problem 108x slower than a CPU to being 89x faster than it. However, identifying the correct patterns and the right optimization level to use for each is very hard to get right, even for experts.			
Most of the article explains, in great detail, sp writing code in a traditional setting, as well as programming. After showing many clear and authors present the above-mentioned DSE to pragmas for the Merlin compiler. AutoDSE for the correct optimization points and values; th performing results "while using 26.38x fewer programs."	s some challenges uniqu frankly easy-to-underst ol, AutoDSE, for the aut uses on automatically d rey mention AutoDSE ca	ue to FPGA and examples, the comatic generation of letecting and applying in achieve similarly	
Given the current status of computing, it is q that Moore's law and Dennard scaling brough improve the speed of computation of problem complexity, programmers will need to find ne certainly pose an attractive way forward. Tool likely help developers tackle the difficult task	t to our field, and in ord as of ever-increasing ma w techniques to aid the is such as the DSE prese	er to continue to gnitude and r processing. FPGAs ented in this article will	
Reviewer: Gunnar Wolf		Review #: CR147606	
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